

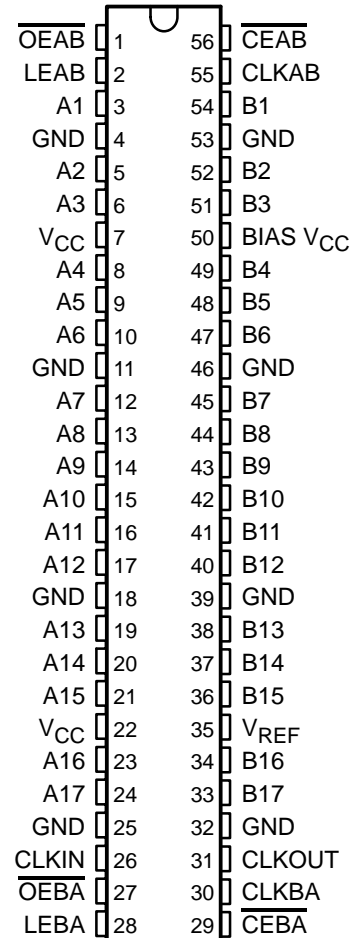
# SN74GTLPH16916

## 17-BIT LVTTTL-TO-GTLP UNIVERSAL BUS TRANSCEIVER WITH BUFFERED CLOCK OUTPUTS

SCES347C – JANUARY 2001 – REVISED JANUARY 2002

- Member of the Texas Instruments Widebus™ Family
- UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, and Clock-Enabled Mode
- TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes
- OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference
- Bidirectional Interface Between GTLP Signal Levels and LVTTTL Logic Levels
- GTLP Buffered CLKAB Signal (CLKOUT)
- LVTTTL Interfaces Are 5-V Tolerant
- Medium-Drive GTLP Outputs (50 mA)
- LVTTTL Outputs (–24 mA/24 mA)
- GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads
- $I_{off}$ , Power-Up 3-State, and BIAS  $V_{CC}$  Support Live Insertion
- Bus Hold on A-Port Data Inputs
- Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DGG OR DGV PACKAGE  
(TOP VIEW)



### description

The SN74GTLPH16916 is a medium-drive, 17-bit UBT™ transceiver that provides LVTTTL-to-GTLP and GTLP-to-LVTTTL signal-level translation. It allows for transparent, latched, clocked, and clock-enabled modes of data transfer. Additionally, it provides for a copy of CLKAB at GTLP signal levels (CLKOUT) and conversion of a GTLP clock to LVTTTL logic levels (CLKIN). The device provides a high-speed interface between cards operating at LVTTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω.



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## description (continued)

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH16916 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL ( $V_{TT} = 1.2\text{ V}$  and  $V_{REF} = 0.8\text{ V}$ ) or GTLP ( $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$ ) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs.  $V_{REF}$  is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using  $I_{off}$ , power-up 3-state, and BIAS  $V_{CC}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS  $V_{CC}$  circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

Active bus-hold circuitry holds unused or undriven LVTTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ( $\overline{OE}$ ) input should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH16916GR	GTLPH16916
	TVSOP – DGV	Tape and reel	SN74GTLPH16916VR	GL916

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**functional description**

The SN74GTLPH16916 is a medium-drive (50 mA), 17-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, clocked, or clock-enabled modes and can replace any of the functions shown in Table 1. Data polarity is noninverting.

**Table 1. SN74GTLPH16916 UBT™ Transceiver Replacement Functions**

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	'245, '623, '645	'863	'861	'16245, '16623	'16863
Buffer/driver	'241, '244, '541		'827	'16241, '16244, '16541	'16825
Latched transceiver	'543			'16543	'16472
Latch	'373, '573	'843	'841	'16373	'16843
Registered transceiver	'646, '652			'16646, '16652	'16474
Flip-flop	'374, '574		'821	'16374	
Standard UBT					'16500, '16501
Universal bus driver					'16835
Registered transceiver with clock enable	'2952			'16470, '16952	
Flip-flop with clock enable	'377	'823			'16823
Standard UBT with clock enable					'16600, '16601
SN74GTLPH16916 UBT transceiver replaces all above functions					

Additionally, the SN74GTLPH16916 allows for transparent conversion of CLKAB-to-GTLP signal levels (CLKOUT) and CLKOUT-to-LVTTTL logic levels (CLKIN).

Data flow in each direction is controlled by clock enables ( $\overline{CEAB}$  and  $\overline{CEBA}$ ), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA), and output enables ( $\overline{OEAB}$  and  $\overline{OEBA}$ ).  $\overline{CEAB}$  and  $\overline{CEBA}$  enable all 17 bits, and  $\overline{OEAB}$  and  $\overline{OEBA}$  control the 17 bits of data and the CLKOUT/CLKIN buffered clock path for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow when  $\overline{CEAB}$  is low, the device operates on the low-to-high transition of CLKAB for the flip-flop and on the high-to-low transition of LEAB for the latch path, i.e., if  $\overline{CEAB}$  and LEAB are low, the A data is latched regardless of the state of CLKAB (high or low) and, if LEAB is high, the device is in transparent mode. When  $\overline{OEAB}$  is low, the outputs are active. When  $\overline{OEAB}$  is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to A to B, except  $\overline{CEBA}$ ,  $\overline{OEBA}$ , LEBA, and CLKBA are used.

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**Function Tables**

**OUTPUT ENABLE†**

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	$B_0^\ddagger$	Latched storage of A data
L	L	L	L	X	$B_0^\S$	
X	L	H	X	L	L	True transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	$B_0^\S$	Clock inhibit

† A-to-B data flow is shown. B-to-A data flow is similar, but uses  $\overline{CEBA}$ ,  $\overline{OEBA}$ , LEBA, and CLKBA. The condition when  $\overline{OEAB}$  and  $\overline{OEBA}$  are both low at the same time is not recommended.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

**BUFFERED CLOCK**

INPUTS				OPERATION OR FUNCTION	MODE
$\overline{CE}$	LE	$\overline{OEAB}$	$\overline{OEBA}$		
X	X	H	H	Z	Isolation
X	X	L	H	CLKAB to CLKOUT	True delayed clock signal
X	X	H	L	CLKOUT to CLKIN	
X	X	L	L	CLKAB to CLKOUT, CLKOUT to CLKIN	True delayed clock signal with feedback path <sup>¶</sup>

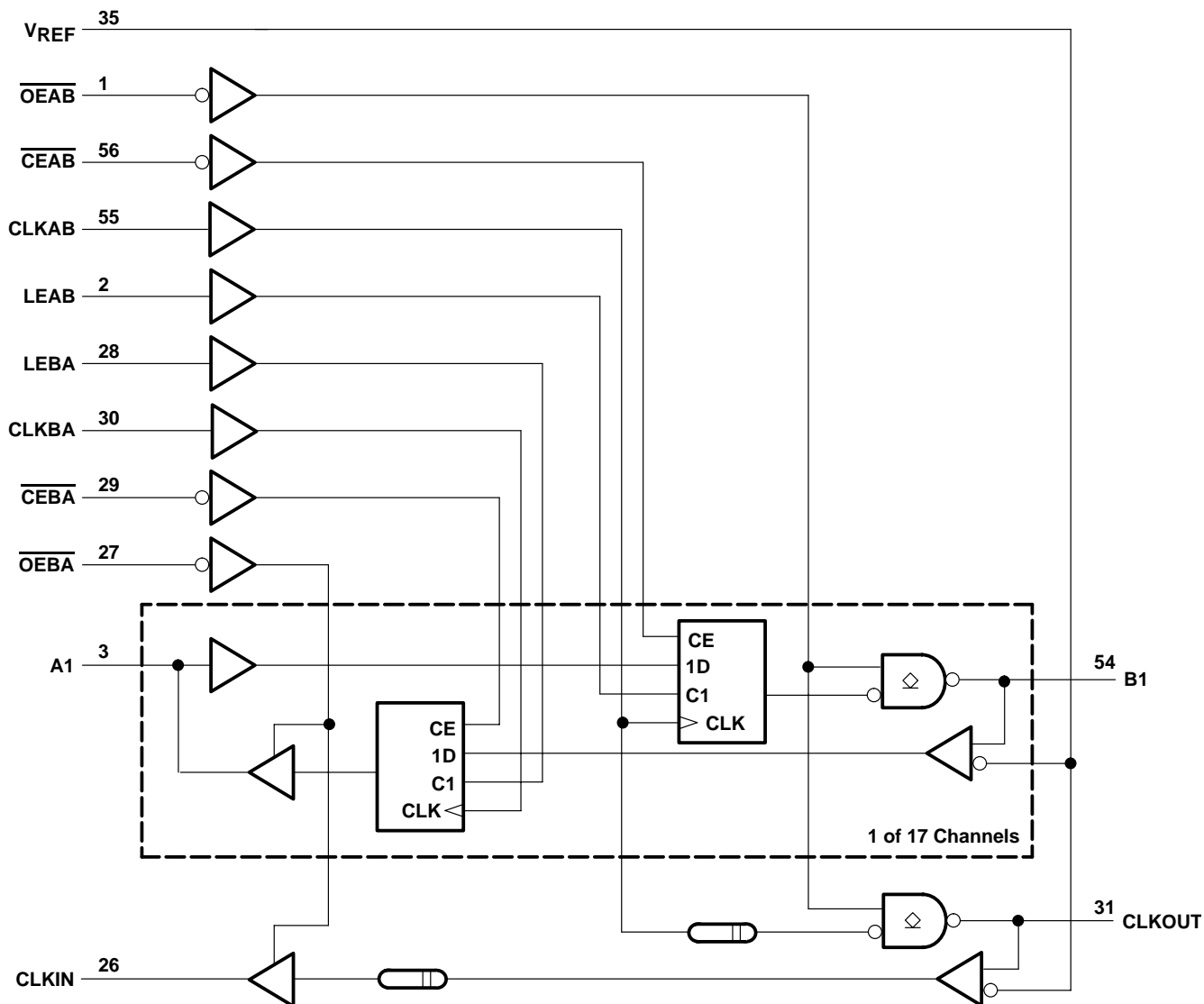
¶ This condition is not recommended.



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**logic diagram (positive logic)**





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**recommended operating conditions (see Notes 4 through 7)**

		MIN	NOM	MAX	UNIT	
$V_{CC}$ , BIAS $V_{CC}$	Supply voltage	3.15	3.3	3.45	V	
$V_{TT}$	Termination voltage	GTLP	1.14	1.2	1.26	V
		GTL	1.35	1.5	1.65	
$V_{REF}$	Reference voltage	GTLP	0.74	0.8	0.87	V
		GTL	0.87	1	1.1	
$V_I$	Input voltage	B port	$V_{TT}$		V	
		Except B port	$V_{CC}$ 5.5			
$V_{IH}$	High-level input voltage	B port	$V_{REF}+0.05$		V	
		Except B port	2			
$V_{IL}$	Low-level input voltage	B port	$V_{REF}-0.05$		V	
		Except B port	0.8			
$I_{IK}$	Input clamp current				-18	mA
$I_{OH}$	High-level output current	A port			-24	mA
$I_{OL}$	Low-level output current	A port			24	mA
		B port			50	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V	
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	20			$\mu$ s/V	
$T_A$	Operating free-air temperature	-40			85	$^{\circ}$ C

- NOTES:
- All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
  - Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS  $V_{CC} = 3.3$  V first, I/O second, and  $V_{CC} = 3.3$  V last, because the BIAS  $V_{CC}$  precharge circuitry is disabled when any  $V_{CC}$  pin is connected. The control and  $V_{REF}$  inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
  - $V_{TT}$  and  $R_{TT}$  can be adjusted to accommodate backplane impedances if the dc recommended  $I_{OL}$  ratings are not exceeded.
  - $V_{REF}$  can be adjusted to optimize noise margins, but normally is two-thirds  $V_{TT}$ . TI-OPC circuitry is enabled in the A-to-B direction and is activated when  $V_{TT} > 0.7$  V above  $V_{REF}$ . If operated in the A-to-B direction,  $V_{REF}$  should be set to within 0.6 V of  $V_{TT}$  to minimize current drain.



# SN74GTLPH16916

## 17-BIT LVTTTL-TO-GTLP UNIVERSAL BUS TRANSCEIVER

### WITH BUFFERED CLOCK OUTPUTS

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#### electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 3.15 V, I <sub>I</sub> = -18 mA				-1.2	V
V <sub>OH</sub>	A port	V <sub>CC</sub> = 3.15 V to 3.45 V, I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V
		V <sub>CC</sub> = 3.15 V, I <sub>OH</sub> = -12 mA		2.4			
		V <sub>CC</sub> = 3.15 V, I <sub>OH</sub> = -24 mA		2			
V <sub>OL</sub>	A port	V <sub>CC</sub> = 3.15 V to 3.45 V, I <sub>OL</sub> = 100 μA				0.2	V
		V <sub>CC</sub> = 3.15 V, I <sub>OL</sub> = 12 mA				0.4	
		V <sub>CC</sub> = 3.15 V, I <sub>OL</sub> = 24 mA				0.5	
	B port	V <sub>CC</sub> = 3.15 V to 3.45 V, I <sub>OL</sub> = 100 μA				0.2	
		V <sub>CC</sub> = 3.15 V, I <sub>OL</sub> = 10 mA				0.2	
		V <sub>CC</sub> = 3.15 V, I <sub>OL</sub> = 40 mA				0.4	
		V <sub>CC</sub> = 3.15 V, I <sub>OL</sub> = 50 mA				0.55	
I <sub>I</sub> ‡	A-port and control inputs	V <sub>CC</sub> = 3.45 V		V <sub>I</sub> = 0 or V <sub>CC</sub>		±10	μA
	B port			V <sub>I</sub> = 5.5 V		±20	
				V <sub>I</sub> = 0 to 1.5 V		±10	
I <sub>BHL</sub> §	A port	V <sub>CC</sub> = 3.15 V, V <sub>I</sub> = 0.8 V			75	μA	
I <sub>BHH</sub> ¶	A port	V <sub>CC</sub> = 3.15 V, V <sub>I</sub> = 2 V			-75	μA	
I <sub>BHLO</sub> #	A port	V <sub>CC</sub> = 3.45 V, V <sub>I</sub> = 0 to V <sub>CC</sub>			500	μA	
I <sub>BHHO</sub>	A port	V <sub>CC</sub> = 3.45 V, V <sub>I</sub> = 0 to V <sub>CC</sub>			-500	μA	
I <sub>CC</sub>	A or B port	V <sub>CC</sub> = 3.45 V, I <sub>O</sub> = 0, V <sub>I</sub> (A port or control input) = V <sub>CC</sub> or GND, V <sub>I</sub> (B port) = V <sub>TT</sub> or GND		Outputs high		50	mA
				Outputs low		50	
				Outputs disabled		50	
ΔI <sub>CC</sub> *			V <sub>CC</sub> = 3.45 V, One A-port or control input at V <sub>CC</sub> - 0.6 V, Other A-port or control inputs at V <sub>CC</sub> or GND			1.5	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3.15 V or 0			4	5.5	pF
C <sub>io</sub>	A port	V <sub>O</sub> = 3.15 V or 0			7	8.5	pF
	B port or CLKOUT	V <sub>O</sub> = 1.5 V or 0			8.5	9.5	
C <sub>O</sub>	CLKIN	V <sub>O</sub> = 3.15 V or 0			6	6.5	pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameter I<sub>I</sub> includes the off-state output leakage current.

§ The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub>max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub>max.

¶ The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub>min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub>min.

# An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.

|| An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.

\* This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

#### hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I <sub>off</sub>	V <sub>CC</sub> = 0,	BIAS V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V		10	μA
I <sub>OZPU</sub>	V <sub>CC</sub> = 0 to 1.5 V,	V <sub>O</sub> = 0.5 V to 3 V,	$\overline{OE} = 0$		±30	μA
I <sub>OZPD</sub>	V <sub>CC</sub> = 1.5 V to 0,	V <sub>O</sub> = 0.5 V to 3 V,	$\overline{OE} = 0$		±30	μA





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**live-insertion specifications for B port over recommended operating free-air temperature range**

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
$I_{off}$	$V_{CC} = 0,$	BIAS $V_{CC} = 0,$ $V_I$ or $V_O = 0$ to 1.5 V		10	$\mu A$
$I_{OZPU}$	$V_{CC} = 0$ to 1.5 V,	BIAS $V_{CC} = 0,$ $V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$		$\pm 30$	$\mu A$
$I_{OZPD}$	$V_{CC} = 1.5$ V to 0,	BIAS $V_{CC} = 0,$ $V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$		$\pm 30$	$\mu A$
$I_{CC}$ (BIAS $V_{CC}$ )	$V_{CC} = 0$ to 3.15 V	BIAS $V_{CC} = 3.15$ V to 3.45 V, $V_O$ (B port) = 0 to 1.5 V		5	mA
	$V_{CC} = 3.15$ V to 3.45 V			10	$\mu A$
$V_O$	$V_{CC} = 0,$	BIAS $V_{CC} = 3.3$ V, $I_O = 0$	0.95	1.05	V
$I_O$	$V_{CC} = 0,$	BIAS $V_{CC} = 3.15$ V to 3.45 V, $V_O$ (B port) = 0.6 V	-1		$\mu A$

**timing requirements over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT} = 1.5$  V and  $V_{REF} = 1$  V for GTLP (unless otherwise noted)**

		MIN	MAX	UNIT	
$f_{clock}$	Clock frequency	CLKAB to B or CLKBA to A		175	MHz
$t_w$	Pulse duration	LEAB or LEBA high		2.8	ns
		CLKAB to B or CLKBA to A	High or low	2.8	
$t_{su}$	Setup time	A before CLKAB $\uparrow$		1.8	ns
		B before CLKBA $\uparrow$		1.5	
		A before LEAB $\downarrow$		1	
		B before LEBA $\downarrow$		2	
		$\overline{CEAB}$ before CLKAB $\uparrow$		1.5	
		$\overline{CEBA}$ before CLKBA $\uparrow$		1.4	
$t_h$	Hold time	A after CLKAB $\uparrow$		0.3	ns
		B after CLKBA $\uparrow$		0.4	
		A after LEAB $\downarrow$		1.1	
		B after LEBA $\downarrow$		0.4	
		$\overline{CEAB}$ after CLKAB $\uparrow$		1	
		$\overline{CEBA}$ after CLKBA $\uparrow$		1	

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$  for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$f_{max}$	CLKAB or CLKBA	B or A	175			MHz
$t_{PLH}$	A	B	2.1		6	ns
$t_{PHL}$			2.1		6	
$t_{PLH}$	LEAB	B	2.2		6.3	ns
$t_{PHL}$			2.2		6.3	
$t_{PLH}$	CLKAB	B	2.2		6.3	ns
$t_{PHL}$			2.2		6.3	
$t_{PLH}$	CLKAB	CLKOUT	3.2		8	ns
$t_{PHL}$			3.2		8	
$t_{en}$	$\overline{OEAB}$	B or CLKOUT	2.6		6.5	ns
$t_{dis}$			2.6		6.1	
$t_r$	Rise time, B outputs (20% to 80%)			2.4		ns
$t_f$	Fall time, B outputs (80% to 20%)			2		ns
$t_{PLH}$	B	A	1.8		5.8	ns
$t_{PHL}$			1.8		5.8	
$t_{PLH}$	LEBA	A	1.7		5.3	ns
$t_{PHL}$			1.7		5.3	
$t_{PLH}$	CLKBA	A	1.8		5.7	ns
$t_{PHL}$			1.8		5.7	
$t_{PLH}$	CLKOUT	CLKIN	2.5		6.5	ns
$t_{PHL}$			2.5		6.5	
$t_{en}$	$\overline{OEBA}$	A or CLKIN	1.5		6.2	ns
$t_{dis}$			1.5		5.9	

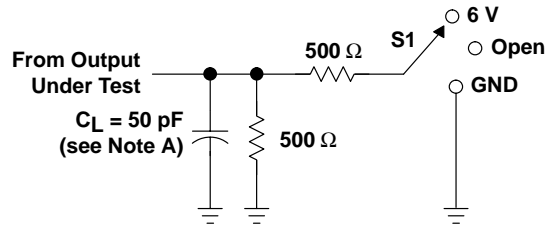
† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .



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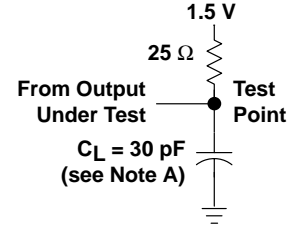
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**PARAMETER MEASUREMENT INFORMATION**

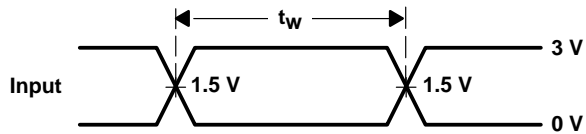


**LOAD CIRCUIT FOR A OUTPUTS**

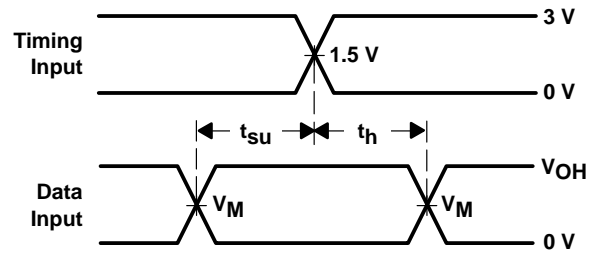
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



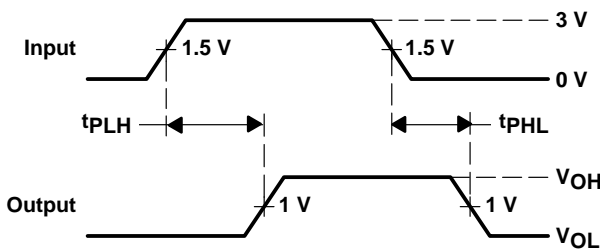
**LOAD CIRCUIT FOR B OUTPUTS**



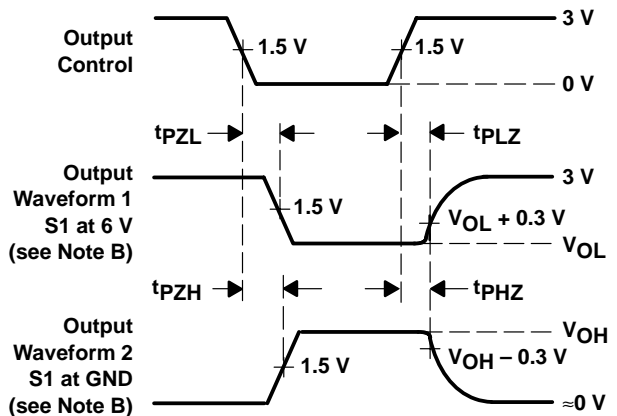
**VOLTAGE WAVEFORMS PULSE DURATION**



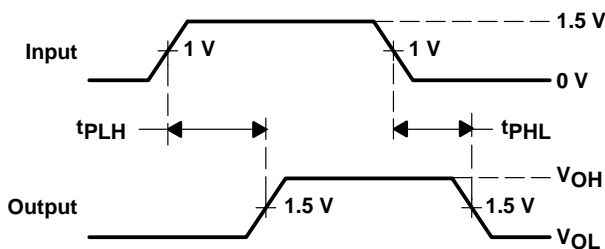
**VOLTAGE WAVEFORMS SETUP AND HOLD TIMES**  
 $(V_M = 1.5 \text{ V for A port and } 1 \text{ V for B port})$   
 $(V_{OH} = 3 \text{ V for A port and } 1.5 \text{ V for B port})$



**VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES (A port to B port)**



**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES (A port)**



**VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES (B port to A port)**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \approx 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \approx 2 \text{ ns}$ ,  $t_f \approx 2 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

# SN74GTLPH16916 17-BIT LVTTTL-TO-GTLP UNIVERSAL BUS TRANSCEIVER WITH BUFFERED CLOCK OUTPUTS

SCES347C – JANUARY 2001 – REVISED JANUARY 2002

## DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See [www.ti.com/sc/gtlp](http://www.ti.com/sc/gtlp) for more information.

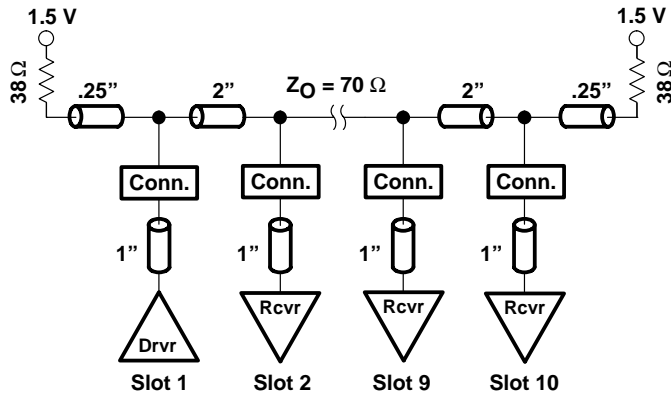


Figure 2. Medium-Drive Test Backplane

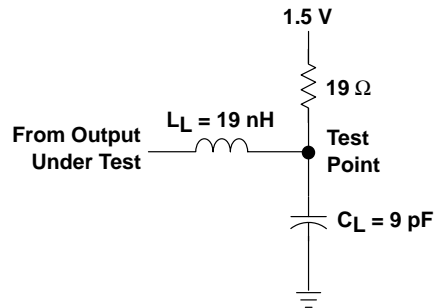


Figure 3. Medium-Drive RLC Network

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$  for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP†	UNIT
$t_{PLH}$	A	B	4.5	ns
$t_{PHL}$			4.5	
$t_{PLH}$	LEAB	B	4.7	ns
$t_{PHL}$			4.7	
$t_{PLH}$	CLKAB	B	4.7	ns
$t_{PHL}$			4.7	
$t_{PLH}$	CLKAB	CLKOUT	6	ns
$t_{PHL}$			6	
$t_{en}$	$\overline{OEAB}$	B or CLKOUT	4.8	ns
$t_{dis}$			4.4	
$t_r$	Rise time, B outputs (20% to 80%)		1.2	ns
$t_f$	Fall time, B outputs (80% to 20%)		2.5	ns

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ . All values are derived from TI-SPIICE models.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

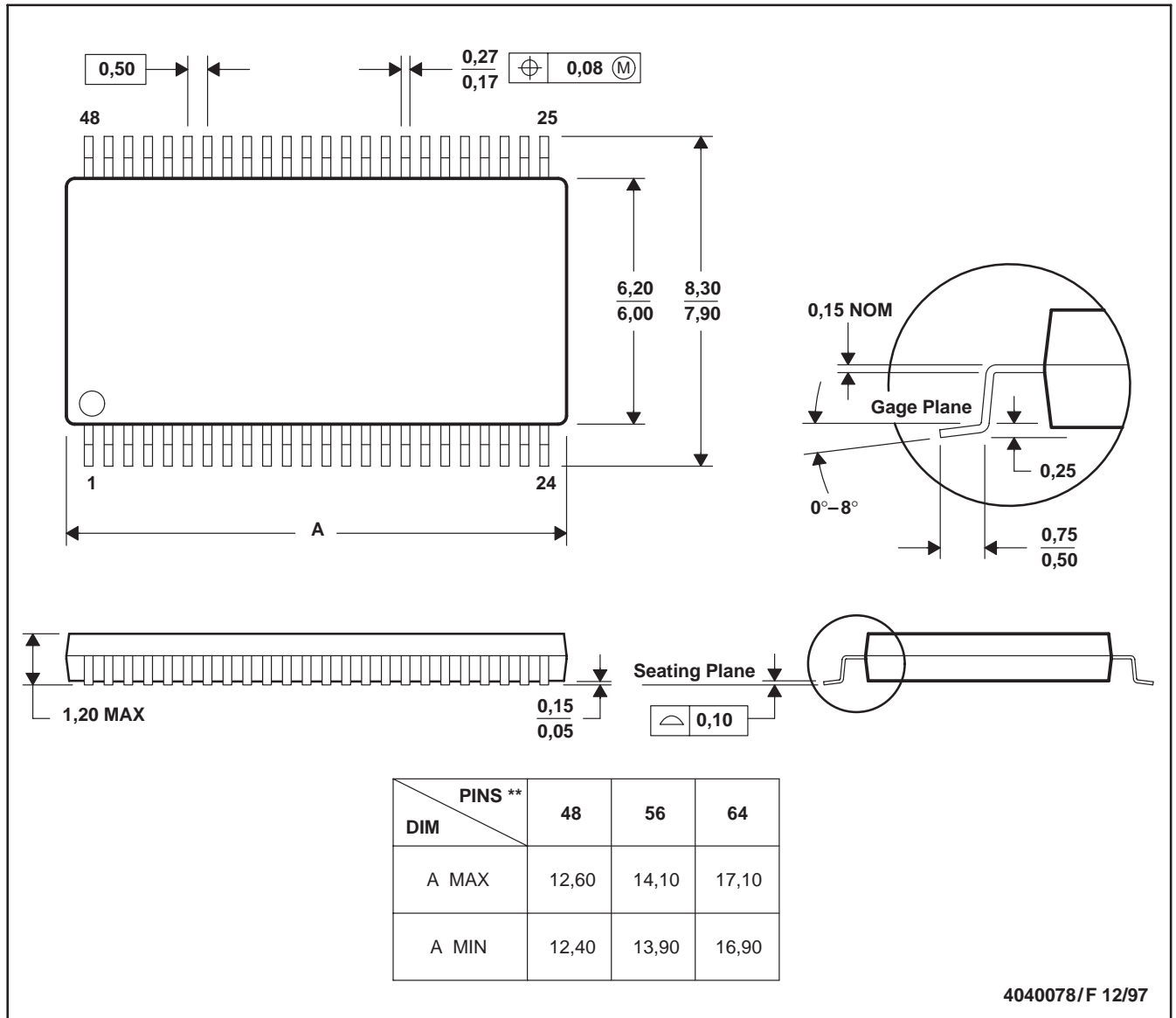


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
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 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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