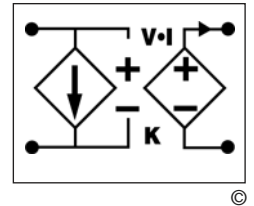




VTM® Chip Transformer

- Isolated 1-50 Vout
- High density
- Small footprint
- ZVS / ZCS Sine Amplitude Converter™
- 3 MHz effective switching frequency
- Surface-mount package
- Low weight
- -55°C to 125°C operation
- 1 μs transient response
- 4.5 million hours MTBF
- Up to 96.5% efficiency



Product Description

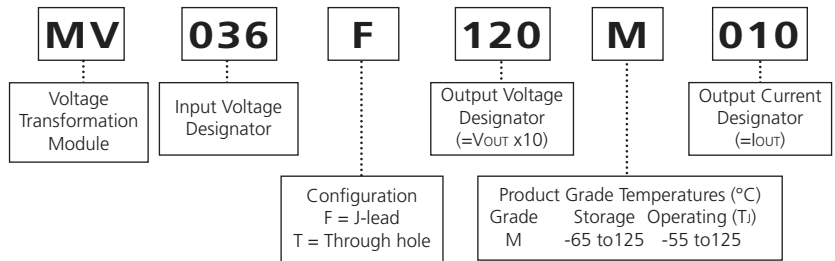
The VTM® transformer is a VI Chip® product that provides extremely fast, efficient, and quiet fixed ratio voltage division (or current multiplication). With twelve voltage division ratios from 1:1 to 1:32, the isolated VTM provides the user with the flexibility to supply up to 100 A or 120 W at any output voltage from 1 to 50 Vdc in a surface mount package occupying ~1 square inch.

The MIL-COTS VTM®s are optimized for use with the MIL-COTS PRM® Regulator to implement a Factorized Power Architecture™ (FPA™). Together, the PRM + VTM chip set provides the full functionality of a DC-DC converter, but with breakthrough performance and flexibility in a rugged, miniature package. The companion PRM for the MV036 family of VTMs is the 28 Vdc input MP028F036M12AL, which operates from an input range of 16-50 Vdc (the data sheet is also available). The VTM can be used as a standalone POL product.

By factorizing the DC-DC power conversion into its essential elements – the VTM’s isolation and transformation, and the PRM’s output voltage control and regulation – and arranging those functions in a sequence that maximizes system performance, FPA offers a fundamentally new and significantly improved approach to power conversion.

The VTM’s fast dynamic response and low noise eliminate the need for bulk capacitance at the load, substantially increasing the POL density while improving reliability and decreasing cost. The low profile VTM (0.265 inches, 6,73 mm) is available with J-leads for surface mount or pins for through hole applications.

Part Numbering Format



Product Status

Part Number	Product Status	Replaced by
MV036F011M100	EOL	none
MV036F015M080	EOL	MVTM36Bx015M080A00
MV036F022M055	EOL	MVTM36Bx022M055A00
MV036F030M040	EOL	MVTM36Bx030M040A00
MV036F045M027	EOL	MVTM36Bx045M027A00
MV036F060M020	EOL	MVTM36Bx060M020B00
MV036F072M017	EOL	MVTM36Bx072M017A00
MV036F090M013	EOL	MVTM36Bx090M013A00
MV036F120M010	EOL	MVTM36Bx120M010A00
MV036F180M007	EOL	MVTM36Bx180M007A00
MV036F240M005	EOL	MVTM36Bx240M005A00
MV036F360M003	EOL	MVTM36Bx360M003A00

## Absolute Maximum Ratings

Parameter	Values	Unit	Notes
+In to -In	-1.0 to 60	Vdc	
	100	Vdc	For 100 ms
PC to -In	-0.3 to 7.0	Vdc	
VC to -In	-0.3 to 19.0	Vdc	
+Out to -Out	Model specific	Vdc	Contact factory
Isolation voltage	2,250	Vdc	Input to Output
Output current	Model specific	A	See Table 1
Peak output current	$1.5 \cdot I_{out}$	A	For 1 ms
Output power	120	W	
Peak output power	180	W	For 1 ms
Case temperature	225	°C	MSL 5
	245	°C	MSL 6
Operating junction temperature <sup>[a]</sup>	-55 to 125	°C	M - Grade
Storage temperature	-65 to 125	°C	M - Grade

### Note:

[a] The referenced junction is defined as the semiconductor having the highest temperature. This temperature is monitored by a shutdown comparator.

## Electrical Specifications

### Input Specs (Conditions are at 36 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Input voltage range	See table 1	36	50	Vdc	
Input dV/dt			1	V/μs	
Input overvoltage turn-on	50.5	54.4		Vdc	
Input overvoltage turn-off		55.5	57.5	Vdc	
Input current			3.5	Adc	Continuous
No load power dissipation	1.5	4.0	7.8	W	Low line to high line

### Output Specs (Conditions are at 36 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Output voltage		See Table 1		Vdc	No load
		$K \cdot V_{IN} - I_o \cdot R_{OUT\ NOM}$		Vdc	Full load
Rated DC current	0		100	Adc	26 - 50 VIN See Table 1
Peak repetitive current			150%	$I_{MAX}$ (A)	Max pulse width 1ms, max duty cycle 10%, baseline power 50%
DC current limit		160%		$I_{NOM}$ (A)	Module will shut down when current limit is reached or exceeded
Current share accuracy		5	10	%	
Efficiency					See Table 2, Page 3
Load capacitance					See Table 2 when used with PRM
Output overvoltage setpoint		110%	115%	$V_{OUT\ MAX}$	
Output ripple voltage (typ)					
No external bypass	50		250	mV	See Figures 2 and 5
10 μF bypass capacitor	2		20	mV	See Figure 6
Effective switching frequency	2.5	3.0	3.6	MHz	Model dependent
Line regulation	0.99K	K	1.01K		$V_{OUT} = K \cdot V_{IN}$ at no load, See Table 1
Load regulation	$R_{OUT\ MIN}$		$R_{OUT\ MAX}$	mΩ	See Table 1
Transient response					
Response time		200		ns	See Figures 7 and 8
Recovery time		1		μs	See Figures 7 and 8

## Electrical Specifications (continued)

## MIL-COTS VTM® Family Part Numbers and Ranges

Part Number	K-Factor	Rated Output Current (A)	No Load Output Voltage (Vdc)		Rout (mΩ)		
			@26 Vin	@ 50 Vin	Min	Nom	Max
MV036F011M100	1/32	100	0.82	1.55	0.5	0.9	1.3
MV036F015M080	1/24	80	1.1	2.0	1.0	1.3	1.5
MV036F022M055	1/16	55	1.63	3.1	1.4	1.75	2.0
MV036F030M040	1/12	40	2.2	4.1	1.45	2.8	3.6
MV036F045M027	1/8	27	3.3	6.2	3.5	6.0	7.1
MV036F060M020	1/6	20	4.3	8.3	5.0	8.0	10
MV036F072M017*	1/5	16.6	6.4*	10	6.0	9.6	12
MV036F090M013	1/4	13.3	6.5	12.5	6.9	11.5	13.9
MV036F120M010	1/3	10.0	8.7	16.6	25	31	40
MV036F180M007	1/2	6.7	14**	25	27.5	43.6	60.0
MV036F240M005	2/3	5.0	17.4	33	49.3	79.0	98.0
MV036F360M003	1	3.3	26	50	140	188	210

Table 1 — VTM part numbers

\* Low line input voltage 32 V

\*\*Low line input voltage 28 V

Part Number	Typical Full Load Efficiency at nom Vout (%)	Typical Half Load Efficiency at nom Vout (%)	Maximum Load Capacitance (μF)
MV036F011M100	89.2	89.3	48128
MV036F015M080	91.9	92.3	27072
MV036F022M055	94	94.5	12032
MV036F030M040	94	94.8	6768
MV036F045M027	94.6	95.6	3008
MV036F060M020	95.3	96.0	1692
MV036F072M017	96.2	96.2	1175
MV036F090M013	96.2	95.5	752
MV036F120M010	94.8	94.9	423
MV036F180M007	95.8	95.2	188
MV036F240M005	95.0	94.8	106
MV036F360M003	96	96	47

Table 2 — Typical efficiency and maximum load capacitance, by part number

## Control Pin Functions

## VC – VTM Control

The VC port is multiplexed. It receives the initial  $V_{CC}$  voltage from an upstream PRM®, synchronizing the output rise of the VTM® with the output rise of the PRM. Additionally, the VC port provides feedback to the PRM to compensate for the VTM output resistance. In typical applications using VTMs powered from PRMs, the PRM's VC port should be connected to the VTM VC port.

The VC port is not intended to be used to supply  $V_{CC}$  voltage to the VTM for extended periods of time. If VC is being supplied from a source other than the PRM, the voltage should be removed after 20 ms.

## PC – Primary Control

The Primary Control (PC) port is a multifunction port for controlling the VTM as follows:

**Disable** – If PC is left floating, the VTM output is enabled. To disable the output, the PC port must be pulled lower than 2.4 V, referenced to -In. Optocouplers, open collector transistors or relays can be used to control the PC port. Once disabled, 14 V must be re-applied to the VC port to restart the VTM.

**Primary Auxiliary Supply** – The PC port can source up to 2.4 mA at 5 Vdc.

Electrical Specifications (continued)

Waveforms

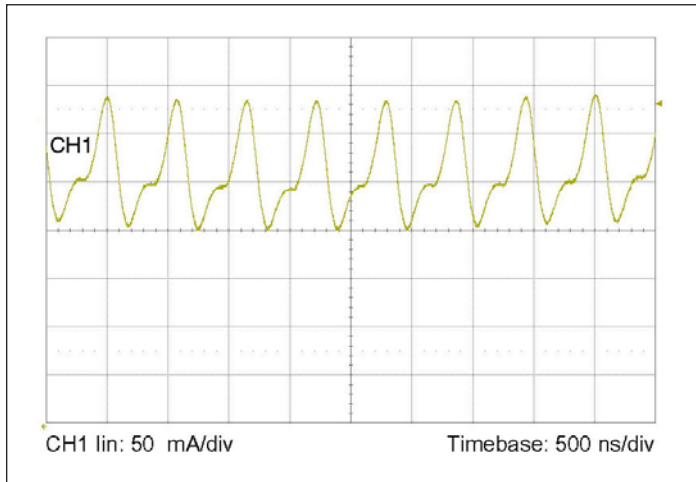


Figure 1 — Representative input reflected ripple current at full load (MV036F120M010).

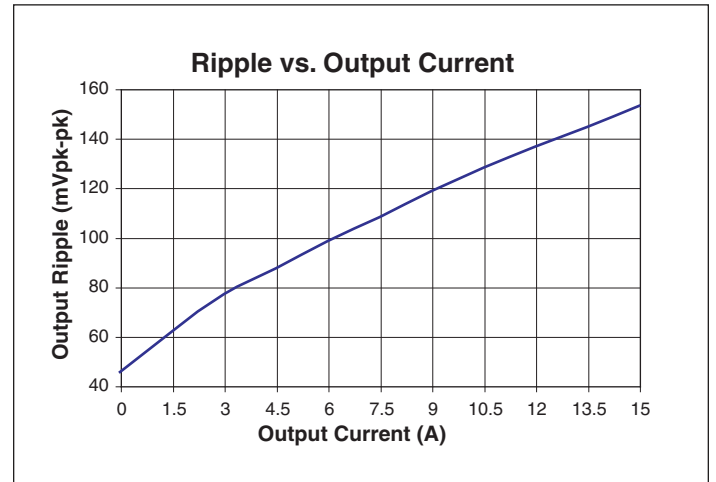


Figure 2 — Sample output voltage ripple vs. output current with no POL bypass capacitance (MV036F120M010).

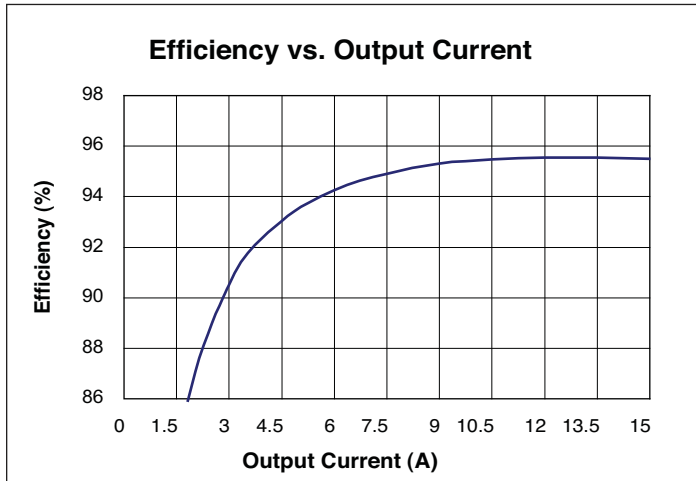


Figure 3 — Representative efficiency vs. output current (MV036F120M010).

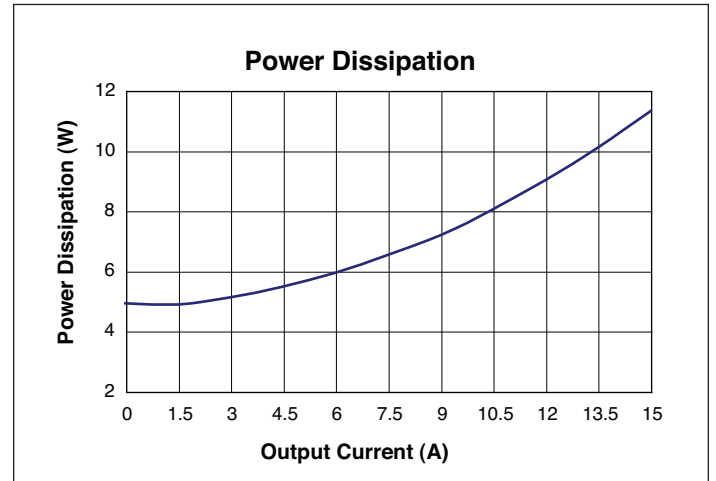


Figure 4 — Example power dissipation vs. output current (MV036F120M010).

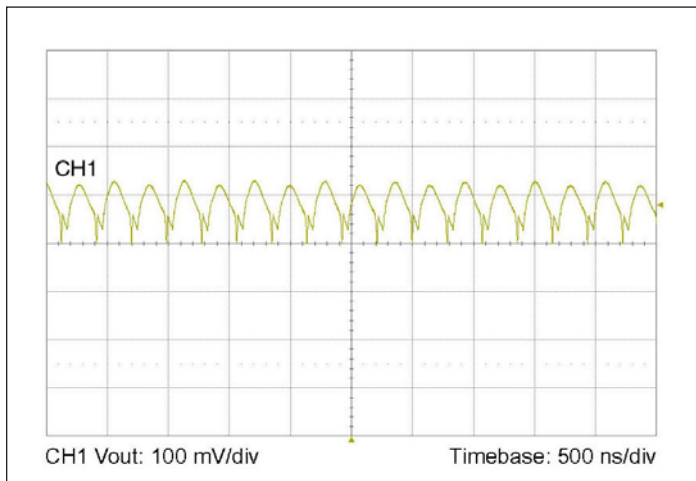


Figure 5 — Sample output voltage ripple at full load; with no POL bypass capacitance (MV036F120M010).

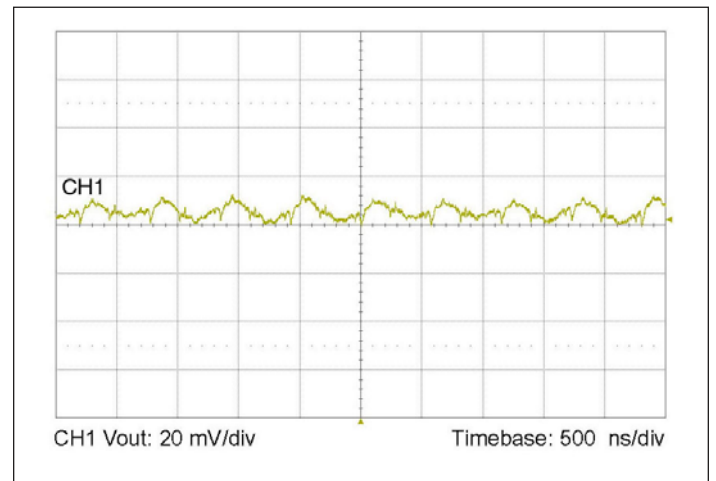


Figure 6 — Sample output voltage ripple at full load with 4.7  $\mu$ F ceramic POL bypass capacitance and 20 nH distribution inductance (MV036F120M010).

Electrical Specifications (continued)

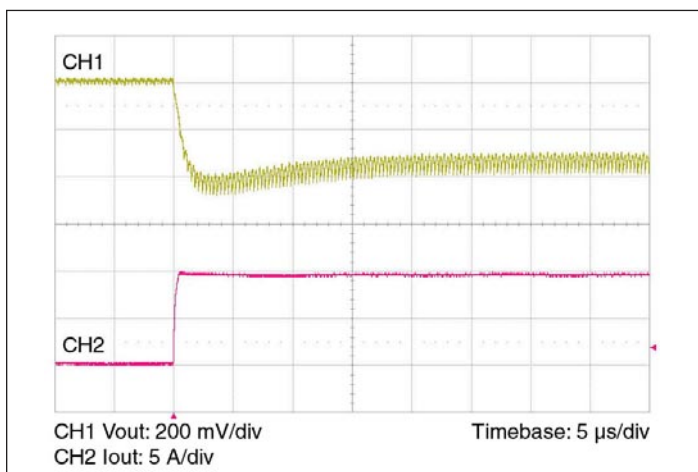


Figure 7 — Example load step with 100 μF input capacitance and no output capacitance (MV036F120M010).

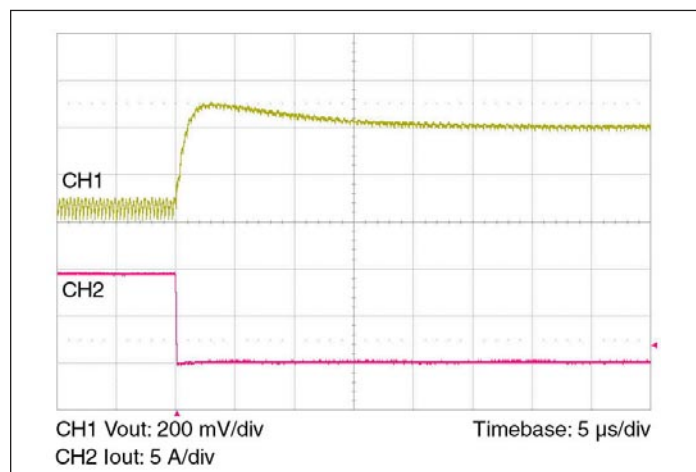


Figure 8 — Example load step with 100 μF input capacitance and no output capacitance (MV036F120M010).

General

Parameter	Min	Typ	Max	Unit	Note
MTBF (MV036F030M040) MIL-HDBK-217F		4,480,000 806,000 631,000		Hours	25°C, GB 50°C NS 65°C AIC
Isolation specifications					
Voltage	2,250			Vdc	Input to Output
Capacitance		3000		pF	Input to Output
Resistance	10			MΩ	Input to Output
Agency approvals		cTUVus			UL/CSA 60950-1, EN 60950-1
					CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable
Mechanical					
Weight		0.53/15		oz /g	See Mechanical Drawings, Figures 10 & 11
Dimensions					
Length		1.28/32,5		in /mm	
Width		0.87/22		in /mm	
Height		0.265/6,73		in /mm	
Thermal					
Over temperature shutdown	125	130	135	°C	Junction temperature
Thermal capacity		9.3		Ws/°C	
Junction-to-case thermal impedance (Rθjc)		1.1		°C /W	
Junction-to-ambient		5.0		°C /W	With 0.25" heat sink*

Auxiliary Pins (Conditions are at 36 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Primary Control (PC)					
DC voltage	4.8	5.0	5.2	Vdc	
Module disable voltage	2.4	2.5		Vdc	
Module enable voltage		2.5	2.6	Vdc	VC voltage must be applied when module is enabled using PC
Current limit	2.4	2.5	2.9	mA	Source only
Disable delay time		6		μs	PC low to Vout low
VTM® Control (VC)					
External boost voltage	12	14	19	Vdc	Required for VTM start up without PRM
External boost duration		10		ms	Maximum duration of VC pulse = 20 ms

**+In / -In DC Voltage Ports**

The VTM® input should be connected to the PRM® output terminals. Given that both the PRM and VTM have high switching frequencies, it is often good practice to use a series inductor to limit high frequency currents between the PRM output and VTM input capacitors. The input voltage should not exceed the maximum specified. If the input voltage exceeds the overvoltage turn-off, the VTM will shutdown. The VTM does not have internal input reverse polarity protection. Adding a properly sized diode in series with the positive input or a fused reverse-shunt diode will provide reverse polarity protection.

**TM – For Factory Use Only**

**VC – VTM Control**

The VC port is multiplexed. It receives the initial V<sub>CC</sub> voltage from an upstream PRM, synchronizing the output rise of the VTM with the output rise of the PRM. Additionally, the VC port provides feedback to the PRM to compensate for the VTM output resistance. In typical applications using VTMs powered from PRMs, the PRM's VC port should be connected to the VTM VC port.

The VC port is not intended to be used to supply V<sub>CC</sub> voltage to the VTM for extended periods of time. If VC is being supplied from a source other than the PRM, the voltage should be removed after 20 ms.

**PC – Primary Control**

The Primary Control (PC) port is a multifunction port for controlling the VTM as follows:

**Disable** – If PC is left floating, the VTM output is enabled. To disable the output, the PC port must be pulled lower than 2.4 V, referenced to -In. Optocouplers, open collector transistors or relays can be used to control the PC port. Once disabled, 14 V must be re-applied to the VC port to restart the VTM.

**Primary Auxiliary Supply** – The PC port can source up to 2.4 mA at 5 Vdc.

**+Out / -Out DC Voltage Output Ports**

The output and output return are through two sets of contact locations. The respective +Out and -Out groups must be connected in parallel with as low an interconnect resistance as possible.

To take full advantage of the VTM, the user should note the low output impedance of the device. The low output impedance provides fast transient response without the need for bulk POL capacitance. Limited-life electrolytic capacitors required with conventional converters can be reduced or even eliminated, saving cost and valuable board real estate.

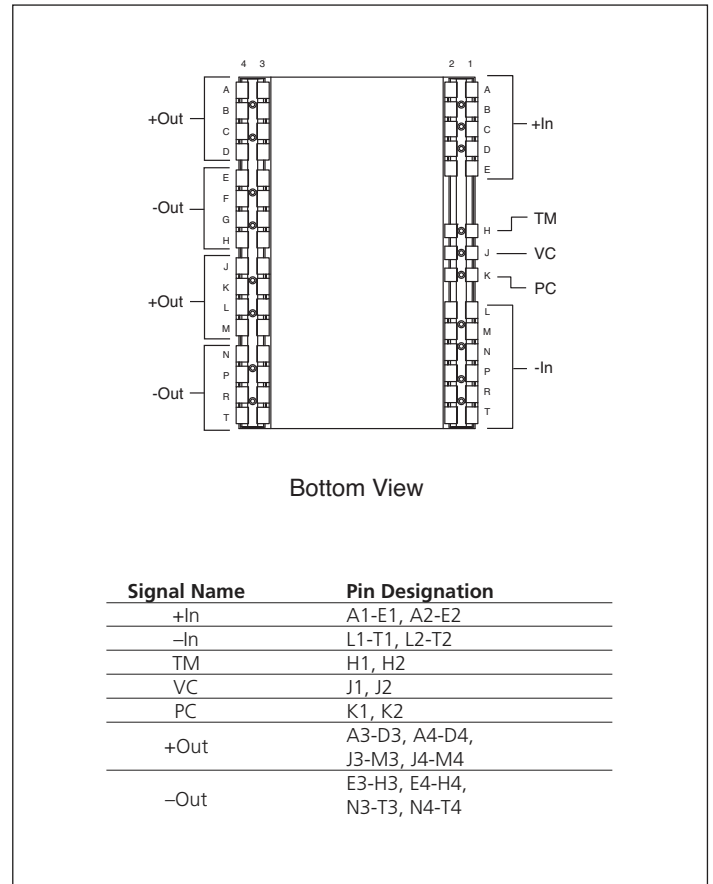


Figure 9 — VTM pin configuration

Mechanical Drawings

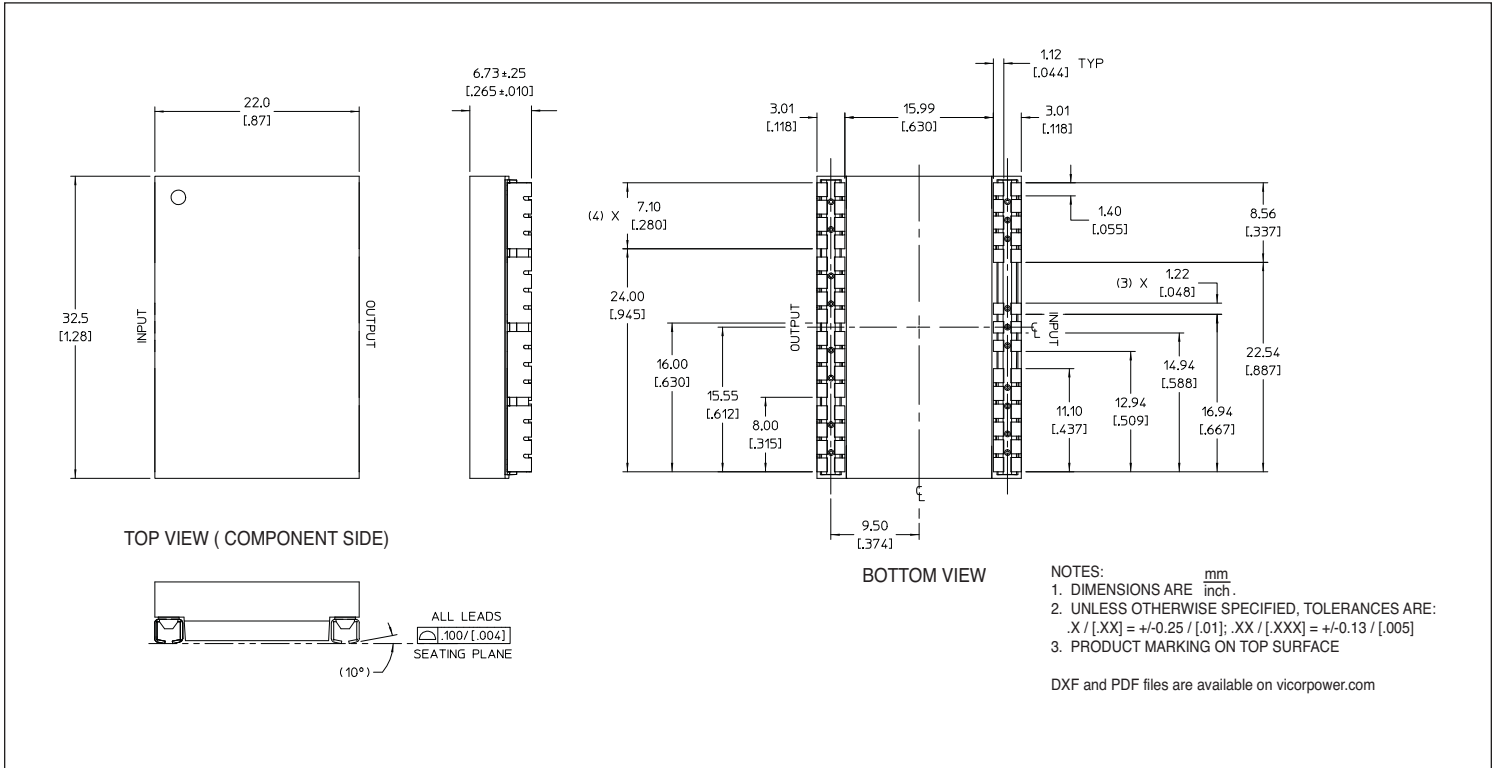


Figure 10 — VTM® mechanical outline

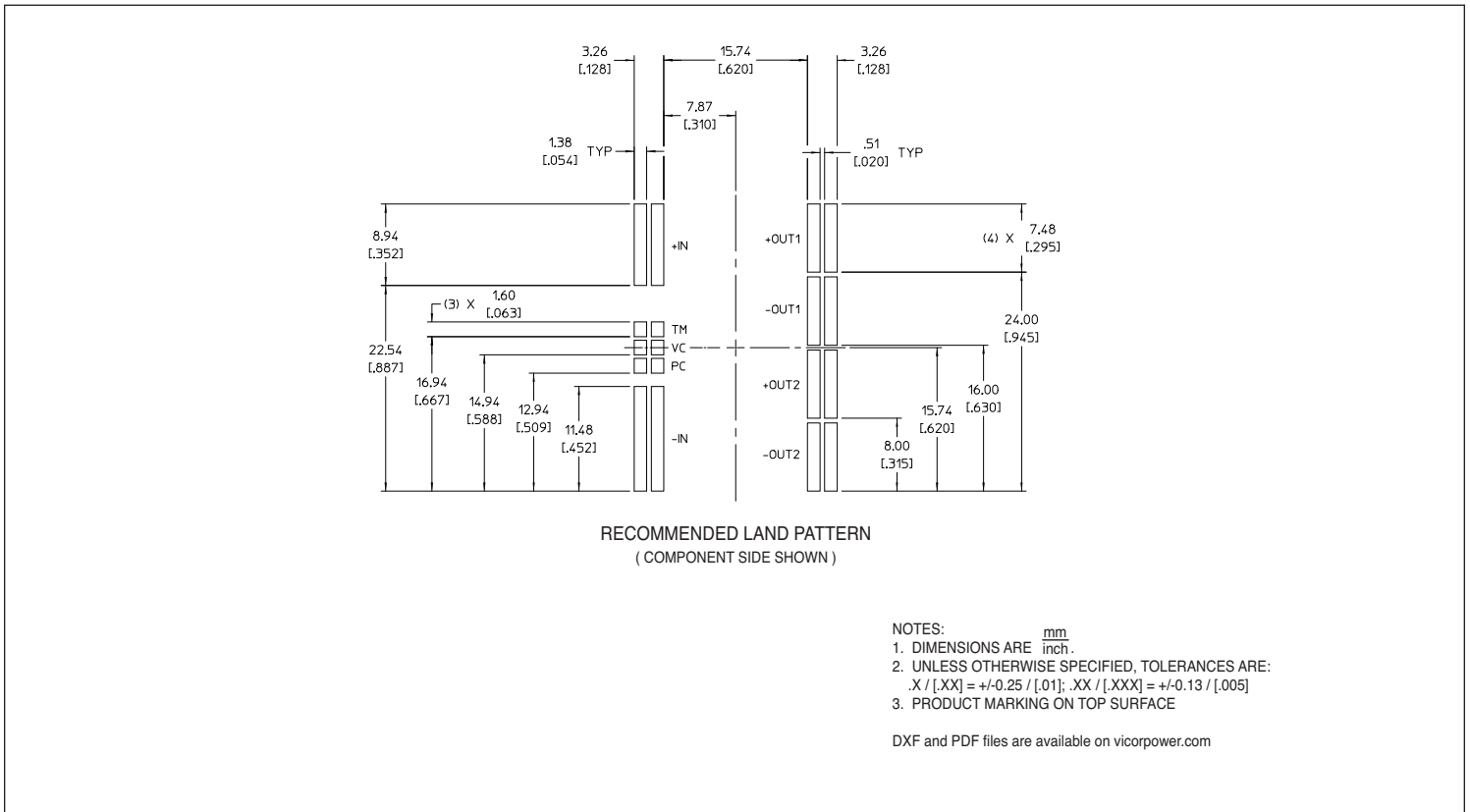


Figure 11 — VTM PCB land layout information

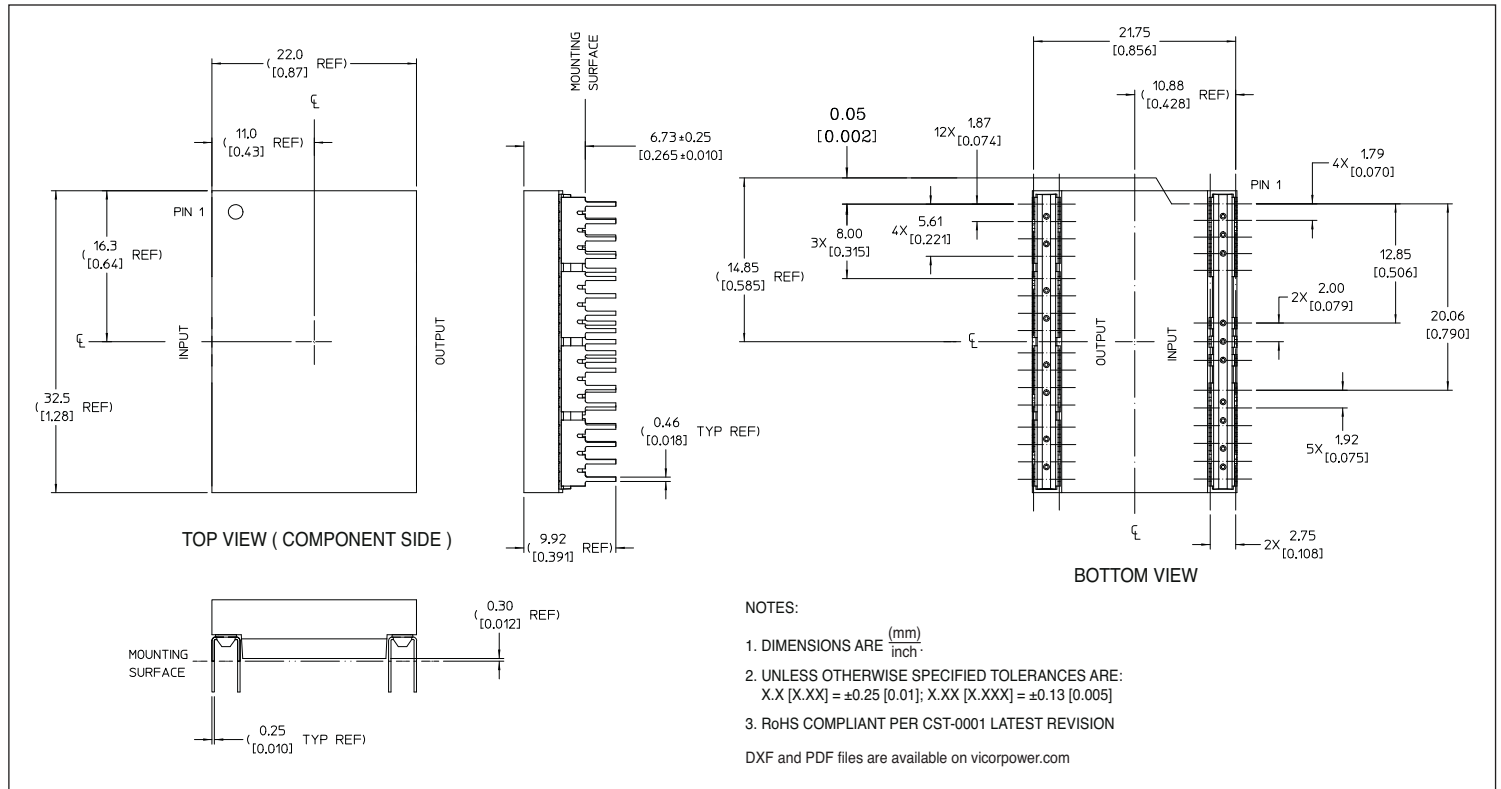


Figure 12 — VTM<sup>®</sup> through-hole mechanical outline

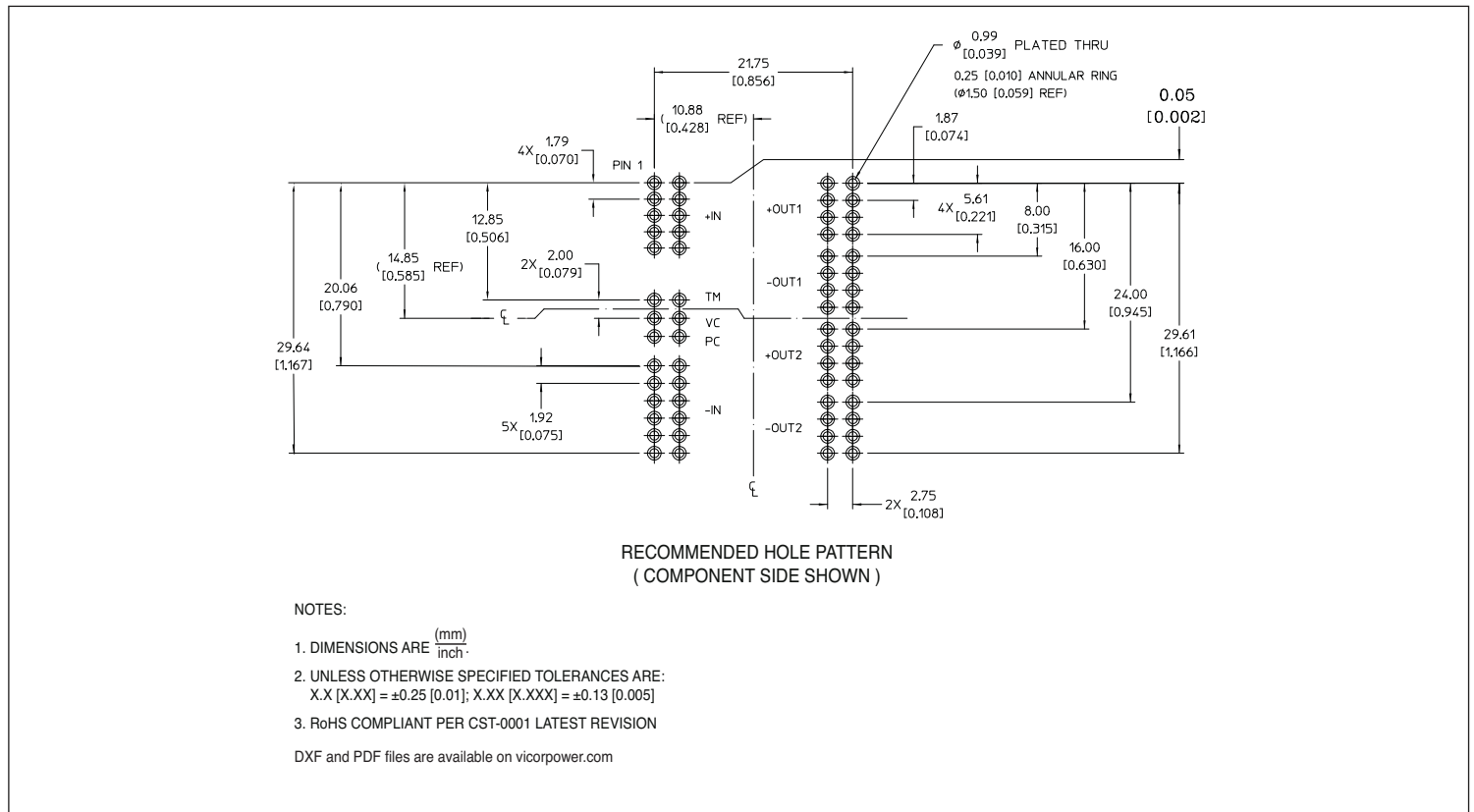


Figure 13 — VTM through-hole PCB layout information



Configuration Options

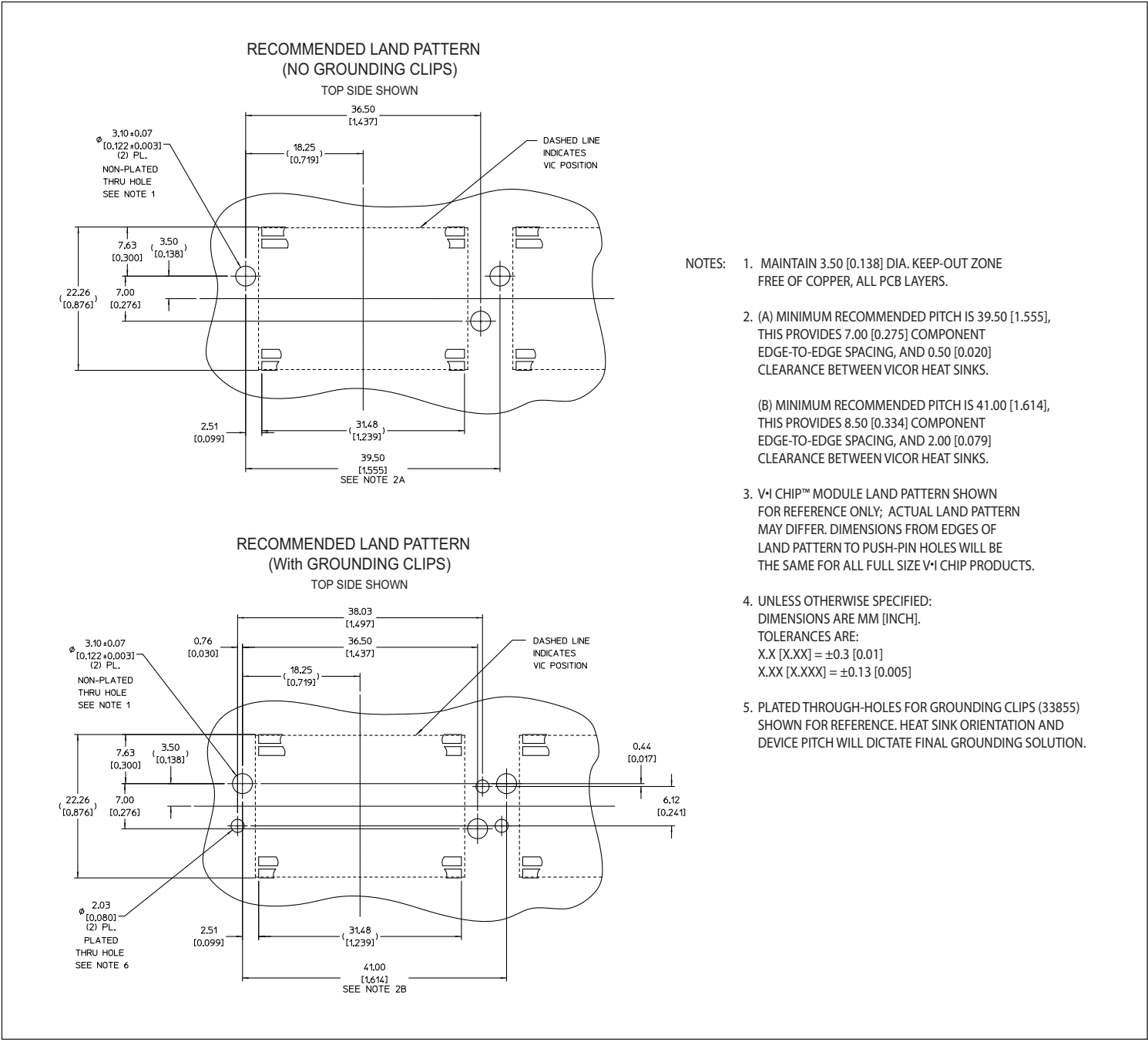


Figure 14 — Hole location for push pin heat sink relative to VI Chip®

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