



# High Speed CMOS 9-Bit Parity Generator/Checker

QS54/74FCT280T

QS54/74FCT1280T

## FEATURES/BENEFITS

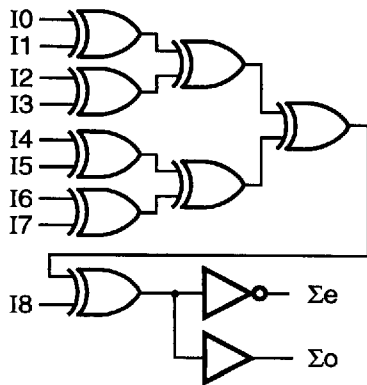
- QSFCT280BT faster than FAST™
- QSFCT1280T has I8 enable, registered outputs
- I<sub>OL</sub> = 48 mA COM, 32 mA MIL
- TTL-compatible input and output levels
- Military product compliant with MIL-STD 883
- 6.3 ns delay, I<sub>x</sub> to Σe for QSFCT280BT
- 2 ns setup, I<sub>x</sub> to reg clock for QSFCT1280BT
- CMOS power levels <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- JEDEC standard pinouts

## DESCRIPTION

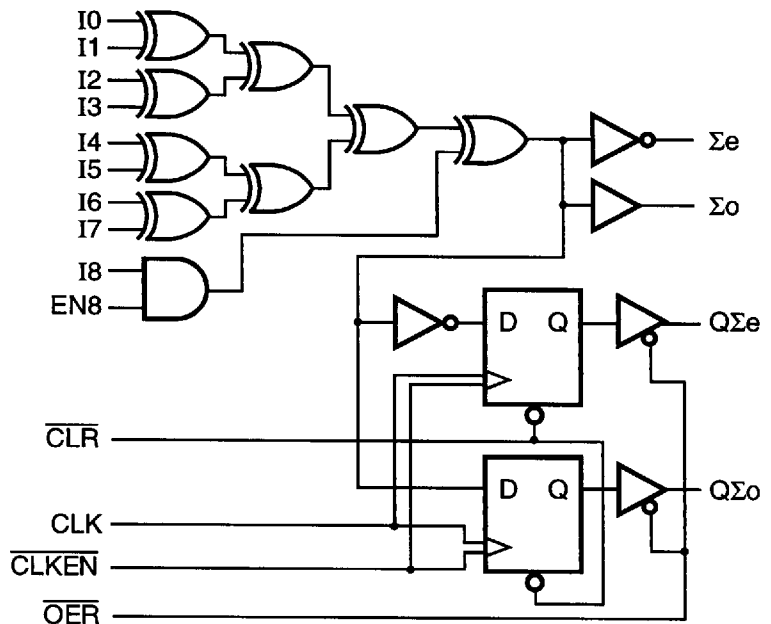
The QSFCT280/AT/BT and QSFCT1280/AT/BT are high-speed CMOS TTL-compatible 9-bit parity generator-checkers. Both odd and even parity outputs are available for generating or checking odd or even parity. The 1280 has I8 enable for parity bit generation and registered odd and even outputs for parity check on the following cycle. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

## FUNCTIONAL BLOCK DIAGRAM

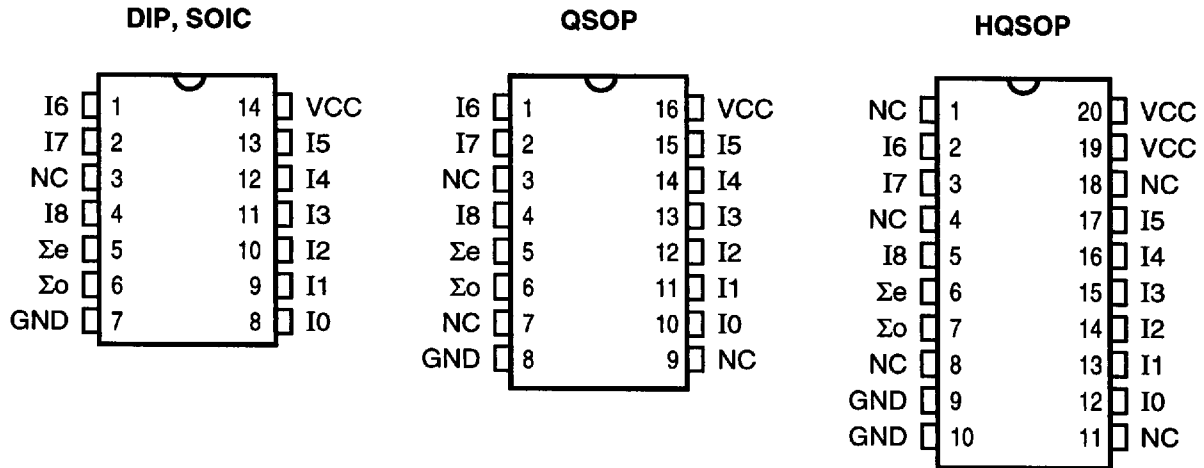
FCT280



FCT1280



**FCT280 PIN CONFIGURATIONS (All Pins Top View)**

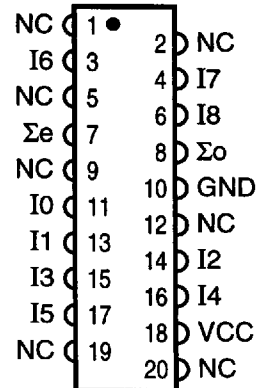


**Note:**  
14-Pin SOIC is 150 mil wide (package code S1).

**PIN DESCRIPTION**

Name	I/O	Description
I8-I0	I	Data Inputs
Σe	O	Even Parity Out
Σo	O	Odd Parity Out

**ZIP**

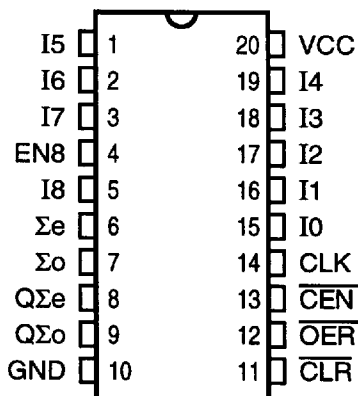


**FUNCTION TABLE**

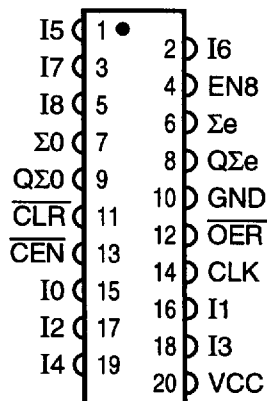
Inputs I8-I0	Outputs		Function
	Σ even	Σ odd	
Number of Bits at TTL High = 0,2,4,6,8	H	L	Parity is Even
Number of Bits at TTL High = 1,3,5,7,9	L	H	Parity is Odd

FCT1280 PIN CONFIGURATIONS (All Pins Top View)

PDIP, SOIC, QSOP, HQSOP



ZIP



PIN DESCRIPTION

Name	I/O	Description
I8-I0	I	Data Inputs
EN8	I	Enable I8
CLK	I	Clock
$\overline{\text{CEN}}$	I	Clock Enable
$\overline{\text{CLR}}$	I	Clear
$\overline{\text{OER}}$	I	Reg. Out Enable
$\Sigma_e$	O	Even Parity Out
$\Sigma_o$	O	Odd Parity Out
$Q\Sigma_e$	O	Reg. Even Parity
$Q\Sigma_o$	O	Reg. Odd Parity

FUNCTION TABLE

Inputs I7-I0	I8	EN8	Outputs	
			$\Sigma_e$	$\Sigma_o$
Number of Bits at TTL High = 0,2,4,6,8	X	L	H	L
	L	H	H	L
	H	H	L	H
Number of Bits at TTL High = 1,3,5,7,9	X	L	L	H
	L	H	L	H
	H	H	H	L

Inputs				Outputs		Function
$\overline{\text{OER}}$	$\overline{\text{CEN}}$	$\overline{\text{CLR}}$	CLK	$Q\Sigma_e$	$Q\Sigma_o$	
H	X	X	X	Hi-Z	Hi-Z	Disable
L	X	L	X	L	L	Clear
L	H	H	↑	$Q\Sigma_{en-1}$	$Q\Sigma_{on-1}$	No Change
L	L	H	↑	$\Sigma_{en-1}$	$\Sigma_{on-1}$	Load $\Sigma_e, \Sigma_o$

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage to Ground .....	-0.5V to +7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to +7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20 mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50 mA
DC Output Current Max. Sink Current/Pin .....	120 mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

**FCT280 CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins (14-Pin Package)	SOIC	QSOP	PDIP	ZIP	Unit
1, 2, 4, 8-13	4	4	5	7	pF
5, 6	6	6	7	9	pF
—	8	8	9	10	pF

**FCT1280 CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1-5, 11-19	4	4	5	7	pF
6-9	6	6	7	9	pF
—	8	8	9	10	pF

**Note:** Capacitance is characterized but not tested.

## QSFCT280T, 1280T

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$I_{IH}$ $I_{IL}$	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OZ}$	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -12 \text{ mA (MIL)}$ $I_{OH} = -15 \text{ mA (COM)}$	2.4 2.4	—	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $I_{OL} = 32 \text{ mA (MIL)}$ $I_{OL} = 48 \text{ mA (COM)}$	— —	—	0.50 0.50	V

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

### POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, \text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}, V_{IN} = 3.4\text{V}, \text{freq} = 0^{(2)}$	—	2.0	mA
$Q_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}, \text{Outputs Open and Enabled}$ One BitToggling @ 50% Duty Cycle Other Inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/ MHz

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ).
3. For flip-flops,  $Q_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4.  $I_C$  can be computed using the above parameters as explained in the Technical Overview section.

## QSFCT280T, 1280T

### FCT280 SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{ pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description		280T		280AT		280BT		Unit
			Min	Max	Min	Max	Min	Max	
tPHLE	Propagation Delay	Com	—	10	—	7.5	—	6.3	ns
tPLHE	I8-I0 to $\Sigma$ even	Mil	—	11	—	9	—	7.5	
tHPLO	Propagation Delay	Com	—	10	—	7.5	—	6.3	ns
tPLHO	I8-I0 to $\Sigma$ odd	Mil	—	11	—	9	—	7.5	

### FCT1280 SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{ pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description		1280T		1280AT		1280BT		Unit
			Min	Max	Min	Max	Min	Max	
tPHLE	Propagation Delay	Com	—	10	—	7.5	—	6.3	ns
tPLHE	I8-I0 to $\Sigma$ even	Mil	—	11	—	9	—	7.5	
tPHLO	Propagation Delay	Com	—	10	—	7.5	—	6.3	ns
tPLHO	I8-I0 to $\Sigma$ odd	Mil	—	11	—	9	—	7.5	
toE	Output Enable Time $\overline{\text{OER}}$ to $Q\Sigma e$ , $Q\Sigma o$	Com <sup>(1)</sup> Mil <sup>(1)</sup>	1.5 1.5	12.5 14	1.5 1.5	10 12	1.5 1.5	7.5 8.5	ns
toZ	Output Disable Time $\overline{\text{OER}}$ to $Q\Sigma e$ , $Q\Sigma o$	Com <sup>(2)</sup> Mil <sup>(2)</sup>	1.5 1.5	8 8	1.5 1.5	7 7	1.5 1.5	6.5 6.5	ns
tCPQ	Clock to Output $Q\Sigma e$ , $Q\Sigma o$	Com Mil	— —	10 11	— —	9 10	— —	7.5 8.5	ns
tCLR	$\overline{\text{CLR}}$ to Output $Q\Sigma e$ , $Q\Sigma o$	Com Mil	— —	13 15	— —	11 13	— —	8 10	ns
tCS	$\overline{\text{CEN}}$ Setup Time $\overline{\text{CEN}}$ to CLK	Com Mil	2.5 2.5	— —	2 2	— —	2 2	— —	ns
tCH	$\overline{\text{CEN}}$ Hold Time $\overline{\text{CEN}}$ to CLK	Com Mil	3 3	— —	2.5 2.5	— —	2 2.5	— —	ns
ts	Data Setup Time Ix to CLK	Com Mil	2.5 2.5	— —	2 2	— —	2 2	— —	ns
th	Data Hold Time Ix to CLK	Com Mil	3 3	— —	2.5 2.5	— —	2 2.5	— —	ns
tw	Clock Pulse Width HIGH or LOW	Com <sup>(2)</sup> Mil <sup>(2)</sup>	7 7	— —	7 7	— —	5 6	— —	ns

**Notes:**

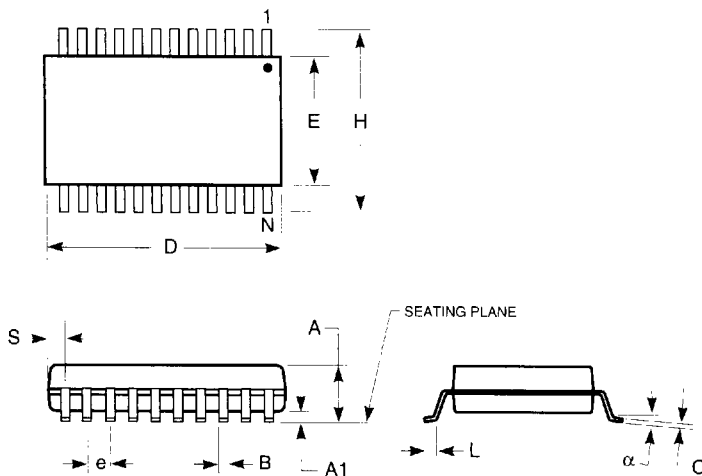
1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.

## PACKAGING INFORMATION

### 150-MIL HQSOP - Package Code H

Hermetic Quarter-Size Outline Package

Ceramic Small Outline Gull-Wing



JEDEC#	TBD			TBD		
DWG#	HSS-20A			HSS-24A		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.070	0.074	0.078	0.070	0.074	0.078
A1	0.008	0.012	0.016	0.008	0.012	0.016
B	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010
D	0.337	0.342	0.350	0.337	0.342	0.350
E	0.150	0.155	0.158	0.150	0.155	0.158
e	0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244
L	0.016	0.025	0.035	0.016	0.025	0.035
N	20			24		
$\alpha$	0°	5°	8°	0°	5°	8°
S	0.056	0.058	0.062	0.031	0.033	0.037

**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition.
5. Lead coplanarity is 0.004 in. maximum.

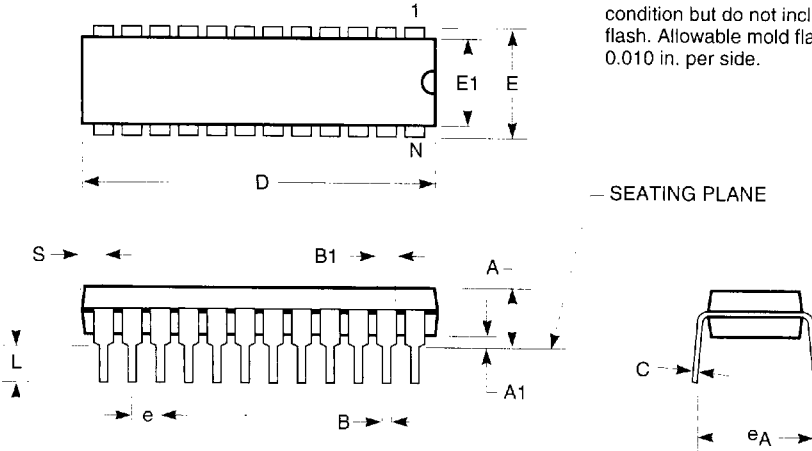
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## PACKAGING INFORMATION

### 300-MIL PDIP - Package Code P Plastic Dual In-line Package

**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010 in. per side.



JEDEC#	MS-001AC		MS001AA		MS-001AE		N/A		MS-001AF		MO-095AH	
DWG#	PD14A		PD16A		PD20A		PT22B		PT24A		PT28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.180
A1	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
B	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020
B1	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.060
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.745	0.765	0.745	0.765	1.020	1.040	1.020	1.040	1.150	1.260	1.345	1.385
E	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
E1	0.240	0.270	0.240	0.270	0.240	0.270	0.240	0.270	0.250	0.280	0.275	0.295
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
<sup>e</sup> A	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380
L	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
S	0.070	0.080	0.020	0.035	0.060	0.070	0.010	0.020	0.025	0.080	0.020	0.040
N	14		16		20		22		24		28	

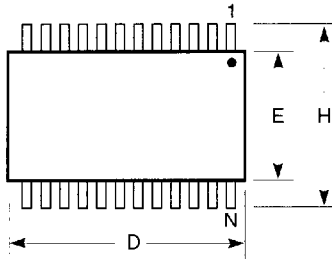
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## PACKAGING INFORMATION

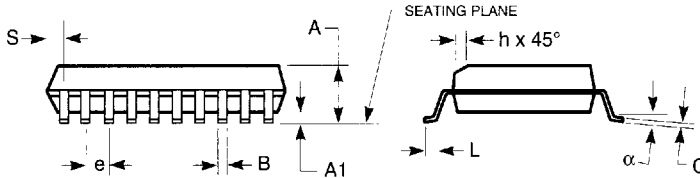
### 150-MIL QSOP - Package Code Q

Quarter-Size Outline Package  
Plastic Small Outline Gull-Wing



**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.

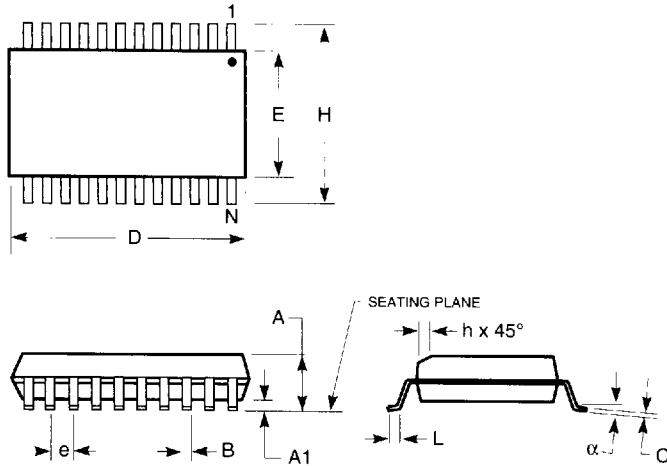


JEDEC#	MO-137AB			MO-137AD			MO-137AE			MO-137AF		
DWG#	PSS-16A			PSS-20A			PSS-24A			PSS-28A		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010
D	0.189	0.193	0.197	0.337	0.341	0.344	0.337	0.341	0.344	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157
e	0.025 BSC			0.025 BSC			0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035
N	16			20			24			28		
$\alpha$	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.006	0.009	0.010	0.056	0.058	0.060	0.031	0.033	0.035	0.031	0.033	0.035

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## PACKAGING INFORMATION

### 150-MIL SOIC - Package Code S1 Plastic Small Outline Gull-Wing



JEDEC#	MS-012AB			MS-012AC		
DWG#	PS-14B			PS-16B		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008
B	0.014	0.016	0.019	0.014	0.016	0.019
C	0.0075	0.008	0.0098	0.0075	0.008	0.0098
D	0.337	0.341	0.346	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157
e	0.050 BSC			0.050 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035
N	14			16		
$\alpha$	0°	5°	8°	0°	5°	8°

**Notes:**

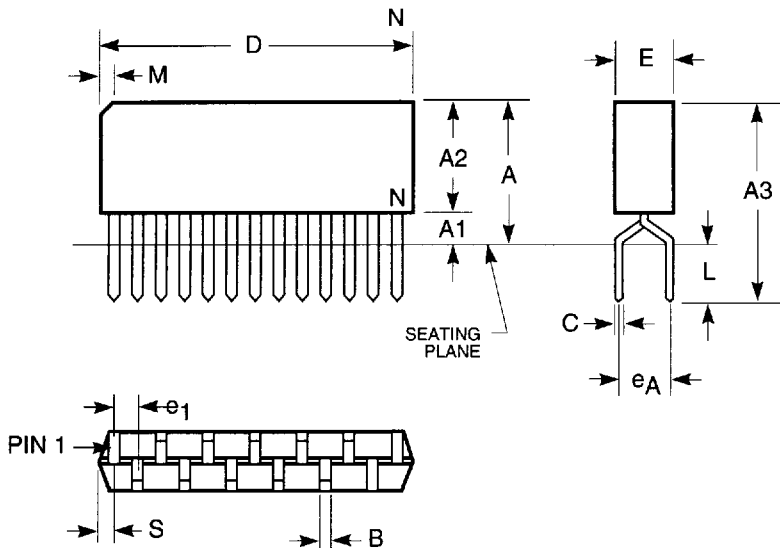
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.

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## PACKAGING INFORMATION

### 300-MIL ZIP - Package Code Z

Zig-zag In-line Packages



JEDEC#	MO-072AB		MO-072AC		MO-072AD	
DWG#	PZ20A		PZ24A		PZ28A	
Symbol	Min	Max	Min	Max	Min	Max
A	0.350	0.400	0.350	0.400	0.350	0.400
A1	0.030	0.070	0.030	0.070	0.032	0.055
A2	0.280	0.340	0.320	0.350	0.335	0.345
A3	0.450	0.550	0.450	0.550	0.460	0.550
B	0.015	0.024	0.015	0.024	0.015	0.024
C	0.008	0.012	0.008	0.012	0.008	0.012
D	1.008	1.030	1.200	1.250	1.409	1.424
E	0.100	0.120	0.100	0.120	0.110	0.120
e1	0.050 BSC		0.050 BSC		0.050 BSC	
eA	0.100 BSC		0.100 BSC		0.100 BSC	
L	0.100	0.150	0.100	0.150	0.110	0.150
M	0.035	0.085	0.035	0.085	0.035	0.085
N	20		24		28	
S	0.018	0.032	0.018	0.032	0.025	0.038

**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010 in. per side.

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